AMENDMENTS TO THE CLAIMS

Please cancel claims 27 and 28 and add new claims 29-31 as follows.

Claims 1-28 (Canceled)

29. (New) A processor for use with a memory, said processor comprising:

a CPU which has an operation state and a stop state, in the operation state the CPU operates in accordance with a clock, and in the stop state the CPU stops operating in accordance with the clock,

wherein when the CPU is in the stop state, data inputted externally of the processor is stored in the memory and the CPU does not always make a transition from the stop state to the operation state due to data being inputted externally of the processor, and

wherein when the CPU is in the operation state, the CPU is operable to process the data which is stored in the memory.

30. (New) A processor , for use with an external processor and a memory, comprising:

a CPU which has an operation state and a stop state, in the operation state the CPU operates in accordance with a clock, and in the stop state the CPU stops operating in accordance with the clock,

wherein when the CPU is in the stop state, data received by the external processor is stored in the memory and the CPU does not always make a transition from the stop state to the operation state due to data being received by the external processor, and

wherein when the CPU is in the operation state, the CPU is operable to process the data which is stored in the memory by the external processor.

31. (New) A data apparatus comprising:

a block having a memory; and

a processor which has an operation state and a stop state, in the operation state the processor operates in accordance with a clock, and in the stop state the processor stops operating in accordance with the clock,

wherein when the processor is in the stop state, the block is operable to receive data and store the data in the memory and the processor does not always make a transition from the stop state to the operation state due to data being received by the block, and

wherein when the processor is in the operation state, the processor is operable to process the data which is received and stored in the memory by the block.